

A New Probing Technique for High-Speed/High-Density Printed Circuit Boards

Kenneth P. Parker
Agilent Technologies
Loveland, CO
kenneth_parker at agilent dot com

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A New Probing Technique for High-Speed/High-Density Printed Circuit Boards

Kenneth P. Parker
Agilent Technologies
Loveland, CO
kenneth_parker at agilent dot com

Abstract

Bullock, in 1987 [Bull87] provided design-for-test (DFT) rules for probing printed circuit boards for In-Circuit testing. Many of these rules stand in good stead even today. However, recent technical advances in operational board speed are leading some to believe that In-Circuit testing cannot be performed on the high-speed sectors of boards soon to be designed. Due to the increasing usage of high-speed circuitry, there is worry in our industry that In-Circuit testing will be marginalized with no good substitute available. It is the purpose of this paper to show how access can be maintained, even on highly dense gigabit logic boards.

1 Introduction

In-Circuit test (ICT) has been an industry workhorse for decades now. Huge numbers of printed circuit boards are tested on In-Circuit testers every day, globally. Important contributions to board testability have been made by the family of Boundary-Scan standards [IEEE01, IEEE99, IEEE03]. Some may have even believed that by concerted use of these standards, the need for ICT probing might disappear. What has happened instead is that the usage of these standards has actually increased the viability of In-Circuit test, where they have been added to the ICT “toolbox”. Boundary-Scan can cover a lot of defects [Park03], while the rest of the ICT toolbox can address the remaining defects [Hird02].

In-Circuit test depends on some amount of direct nodal contact (or “access”) via a “bed-of-nails” fixture as depicted in Figure 1. This allows the ICT system to switch in any of a set of resources needed to perform a test. This may be as simple as making a two-wire measurement of a resistor value, or setting up hundreds of digital drivers and comparators, driven by a digital test sequencer for performing a digital test (including Boundary-Scan tests). Here are some reasons why nodal access may be limited:

1. Density of devices, pins and traces on the board.
2. Some traces may never appear on a probe-able surface layer.
3. Standard access points interfere with board performance.

Items 1 and 3 in this list are the subject of this paper.

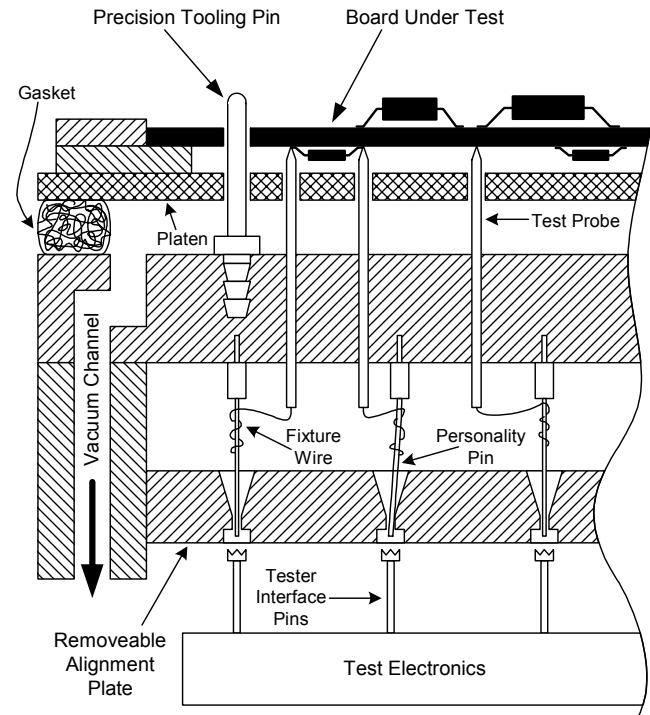


Figure 1: Cutaway drawing of a portion of an ICT fixture.

2 Probing Boards

Rules related to probing are driven by the need to reliably make hundreds or thousands of probe contacts with each board. This must be accomplished many thousands of times during the life of an ICT fixture. If even one probe fails to make contact, a board may not be testable, or worse, tested incorrectly. This has generated industry norms for board probing; what you could call “Design for Probe-ability”.

Probes can be thought of as little spears that are aimed at targets on a board. Bullock [Bull87] gave rules for forming such targets, or using “natural” targets that may exist on a board. One common natural target is a via that connects segments of a trace on different board layers. However, as trace dimensions continue to shrink along with device and pin sizes, the targets we want to probe become smaller to the point where they cannot be hit reliably. Thus there is a practical lower bound on

target size. Bullock cited 35 mil (0.89 mm) round targets as a reliable size. Today, some are pushing the limits down to 26 mils (0.66 mm) and even lower, at greatly increased expense and risk to probing success. Note that a 35 mil round target has an area of 962 mil² while an 0204 surface mount device has an area of 800 mil². Thus a test access point can consume an area that could have contained a device. But worse, consider that PC trace widths used for controlled impedance boards have very strict line width and space requirements. In modern high-speed designs, trace widths and spaces as small as 3 mils (0.076 mm) may be used. At gigabit data transmission rates, there is little tolerance for deviations in these specifications. Thus, asking a designer to add a 35-mil target to a 3 mil wide trace is not likely to be met with friendly acquiescence.

3 High-Speed Design Rules

High-speed design rules impose a new level of complexity on designers as they lay out boards. Typically, for single-ended signals, traces must have a certain width, thickness, height above a ground plane and proximity to grounds in the same plane. The dielectric constant of the board must be carefully controlled. All of this adds together to create a trace with characteristic impedance typically from 28 to 100 ohms. For example, the RAMBUS layout rules (see www.rambus.com) show a layout given in Figure 2, which achieves 28 ohms. At this lower impedance, the traces are wider, but still only about half the width of a preferred probe target. Placing a 35 mil round target on this trace would add a significant capacitance to ground at that point, and effectively lower the impedance there. This creates an “impedance bump” in the signal path that will reflect some of the wave front signal, degrading the signal quality.

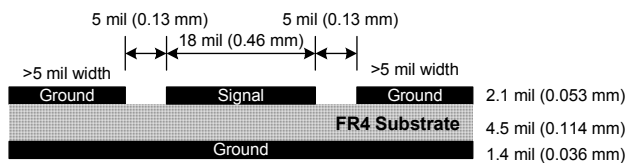


Figure 2: A RAMBUS layout specification for a single-ended trace.

Another problem that probe targets introduce is that of causing trace separations and bends. Ideally, all differential traces would be identical much as in the top case in Figure 3 with a minimum of corners and bends. The separation of the traces is a fundamental determinant of the characteristic impedance of a differential pair. For example, using differential design parameters from the new PCI Express (see www.pcisig.com/specifications) high-speed bus standard, we can achieve 100-ohm differential impedance with 5-mil line width and space.

If we decide to add probe targets for testing, we are

forced to spread apart the traces and introduce bends, either symmetrically or asymmetrically as in Figure 3. Spreading the traces could easily increase the differential impedance to 120 ohms.

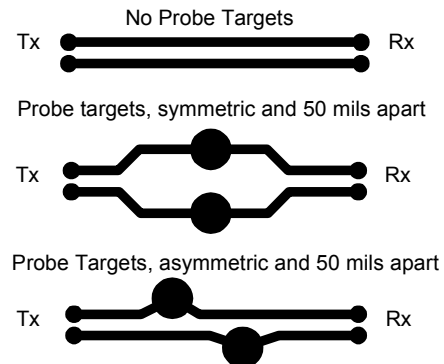


Figure 3: Differential pairs with and without probe targets.

The 50-mil (minimum) target separation is again from Bullock [Bull87] and is due to the size of the probes themselves. Clearly the problem is multiplied if one needs to add probe targets to many pairs of traces traveling across a board in parallel. Each additional target will cause bends and separations in the probed traces, and additional bends in those traces nearby that need to be moved as well, as in Figure 4.

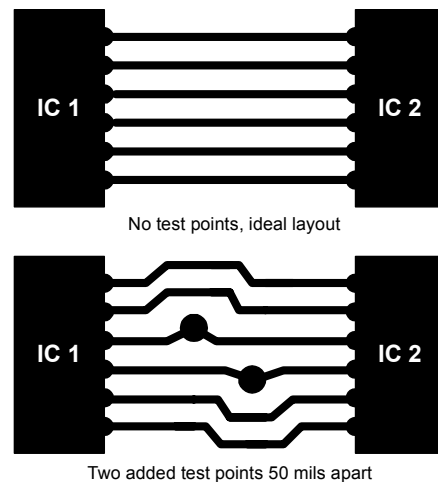


Figure 4: Dense layouts must be redesigned to add test points.

These perturbations in the signal paths cause great concern among designers. They feel they are being asked to take significant design risks in support of test.

4 Won't Boundary-Scan Fix This?

One great contribution of Boundary-Scan is that it removes much need for direct circuit probing. In essence, Boundary-Scan moves the test points into the silicon perimeter of the ICs. With the advent of IEEE Std 1149.4

[IEEE99] we could even test a lot of analog discrete components without direct circuit contact.

There is even the new IEEE Std 1149.6 [IEEE03] formulated to test “advanced” I/O and the differential and AC-coupled structures we are now seeing on boards. Surely this would remove the need for any probe targets.

Unfortunately, no; this is not the situation. Consider a case where 1149.6 has been implemented in some high-speed ICs, for example, in a PCI Express structure. PCI Express uses differential data transport, and AC coupling. The rules call for the AC coupling to be located on the driver side of a transmission path. Many times, a PCI driver will exist on one board and the intended receiver on another. This could leave us with a board like that in Figure 5.

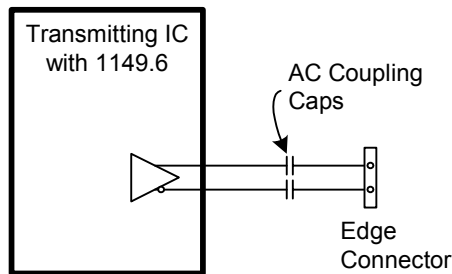


Figure 5: Differential driver, AC-coupling and edge connector.

For a tester to be able to use the 1149.6 capability, it will need access to the two differential signals. One approach would be to fixture a mating connector¹ to the board’s edge connector. However, most testers, including ICT and benchtop Boundary-Scan testers, cannot directly listen to AC-coupled signals. So some additional fixture electronics are also needed to capture the AC signal during test. However, if an ICT did have direct nodal access to the two signals between the IC and the capacitors, then it could listen to the DC voltage levels of the IC during test. In a secondary test² the ICT could stimulate the two nodes to test the capacitors and the connector pins. So we as test engineers would very much like to gain direct nodal access to those two traces. The question: how to enlist our friends, the designers? And of course, we have many other places we’d like to get access to as well. What we need is a “layout-independent” means of adding probe targets as viewed by a board designer. Layout-independence means a designer can lay out traces and later come back and add test points without need of changing that layout.

¹ This is an unpopular approach in high-volume manufacturing since the automatic insertion of a connector is difficult (expensive) to do reliably.

² This portion of test would be done with a TestJet® type of capacitive connector test. The series capacitors would be tested as a byproduct of this. This test does not need a mating connector.

5 Inverting the Probing Paradigm

The ICT bed-of-nails fixture has been an accomplished technology for decades. We know how to assure that thousands of spear-like probes will successfully hit their targets on the board, day after day.

But, what if we were to invert this model? What if the board contained the probe, and the fixture contained the target? Imagine for a moment that you could somehow place a tiny probe on a board and you had a 35-mil target in your fixture. The tolerances and accuracies you currently know how to manage are all still applicable. In principle, this could work. The question is, how to place a probe on a board, and, how will it affect the board’s performance? And of course, it’s got to be inexpensive, reliable and repeatable.

6 Bead Probes

Placing a new component on a board, one that is similar in width to the trace we want to contact, would be difficult. However, we can engineer a very small hemi-ellipsoid of solder, what we call a “bead probe”, detailed below. This bead would lie on top of a trace, aligned to its width and following the trace for 4 to 6 times its width. This bead would be only a few mils tall, clearing the surrounding solder mask by several mils.

6.1 The Bead Probe and Fixtured Target

End and side sectional views of solder bead are shown in Figure 6. The size and shape of the bead is determined by the volume of solder, the area of exposed copper and surface tension while it is molten.

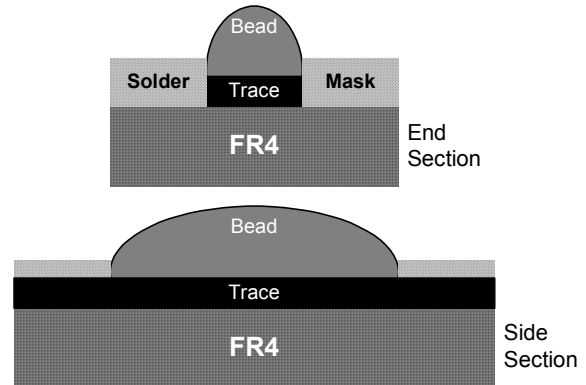


Figure 6: End and side sectional views of a bead probe.

The bead protrudes above the solder mask that is typically only a mil or two thick. When the fixture is activated, bringing the board into contact with the fixture probes, the probe targets situated in the fixture that will contact the bead probes. The fixture targets are round, flat-faced spring-loaded “probes” we often use for probing pointed objects such as through-hole pins. Now their role is reversed to being the target. See Figure 7.

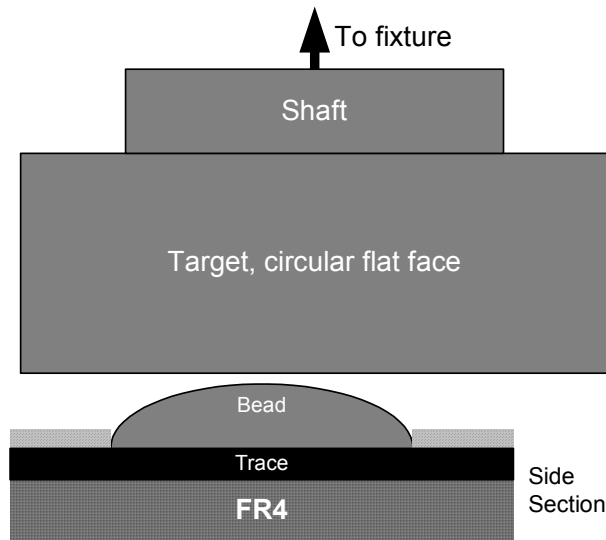


Figure 7: Side view of bead probe and target.

Note that the inevitable registration errors become lateral translation errors, where the bead probe and the target are not perfectly centered. The errors that occur are the same we have been handling for many years.

Assuming the target is 35 mils, the bead in Figure 7 appears to be about 17 mils long. From Figure 6 one would surmise the bead is 6 mils wide and maybe 4 mils tall. It turns out that these (or similar) dimensions are critical to the performance of bead probes. This will be explained in section 7. Suffice it to say here that bead probes are very small, nearly invisible to the naked eye, and, there is such a thing as a bead that is too big.

6.2 Fabricating a Bead Probe

A bead probe is manufactured using the same steps that all other solder features follow. The solder mask is opened up over the trace where we want a bead. When solder flows and then freezes, it will wick up onto the copper trace due to the affinity of solder for copper and lack of affinity for the mask. At this scale, surface tension will completely overwhelm gravity, causing the bead to have a curved surface. The solder mask opening defines the outside dimensions of the bead.

The height of the bead is controlled by two factors. First, by volume, a typical solder paste is roughly 50% flux, which will vaporize during reflow. Thus roughly 1/2 the volume of paste will be deposited as solder. The solder stencil aperture is sized to assure that enough solder is deposited to later “bead up” via surface tension to a height that exceeds the surrounding mask. An example stack up of trace outline, solder mask and stencil holes is shown in Figure 8.

The solder mask hole is an obround hole (rectangular with rounded ends) of width W and length L center to center as shown. The width should be equal to or

less than the width of the trace. The length should run in the same direction as the trace. Choice of width and length is given in the next section. The area of the obround hole, which exposes copper, is $WL + \pi(W/2)^2$.

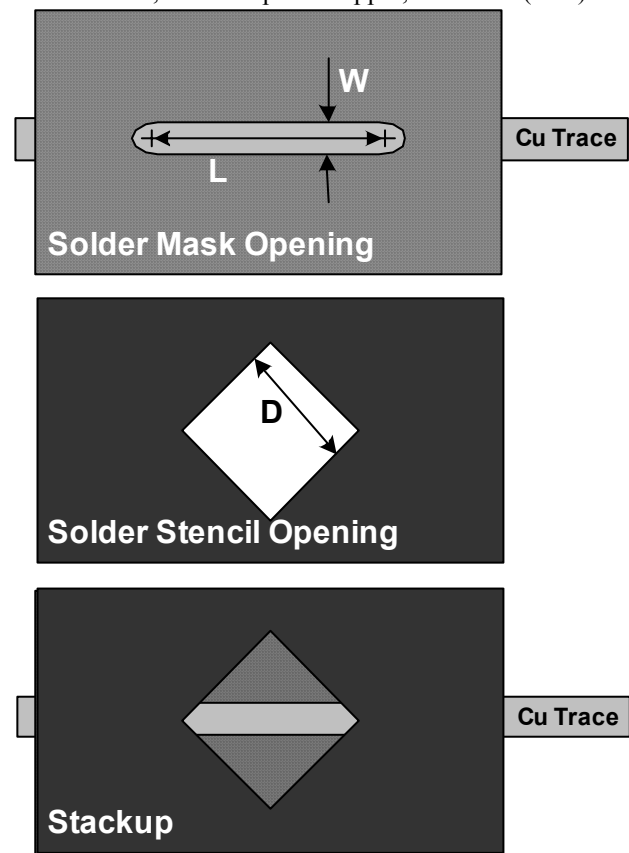


Figure 8: Board, solder mask and solder stencil layer stack up for a bead probe.

The solder stencil hole is a square (side length D) rotated 45 degrees to the trace and centered on the bead location. This hole is larger in area, D^2 , than the mask hole. The rotation maximizes the area of copper that will receive solder paste, while the square is a preferred geometry for reliable stenciling. Some paste will be applied to the solder mask, but this paste will flow onto the copper when melting. The thickness T of the stencil will also determine the amount of solder paste that is applied. The paste volume applied to the board will be TD^2 , which after vaporizing the flux will yield $TD^2/2$ volume of solder.

Given W , L , D and T , we can calculate the approximate height H of the resulting bead as follows. Divide the solder volume by the exposed copper area, or:

$$H \approx (TD^2/2) / (WL + \pi(W/2)^2)$$

If we are given W , H , D and T , then we can calculate the approximate length of the bead as:

$$L \approx ((T*D^2/2) / (H * W)) - \pi W/4$$

7 Theory of Operation

ICT bed-of-nails probing works by using sharp pointed probes to hit targets on a board. Consider a spear-shaped probe contacting a solder-covered target. The spring-force of the probe will force the sharp point into the solder for some distance. This distance is governed by the spring force and the yield strength of solder. Yield strength for solder (leaded and lead-free) is about 5000 pounds per square inch.

As the spear point first touches the solder and any oxide or contaminants on its surface, the area of the point is not large enough to support the spring force, causing the solder to yield. The point of the probe begins to enter the solder, displacing any oxide or contaminants. At the probe tip continues to enter the solder, it has an increasing cross-sectional contact area. At some time this area will be large enough to support the spring force, and the probe no longer displaces solder so the probe does not travel any further into the solder.

Bead probes also show displacement of solder when contacted by a flat-faced probe. They get a flattened head as shown in Figure 9. This flattening displaces oxide and contaminants and provides good electrical conductivity.

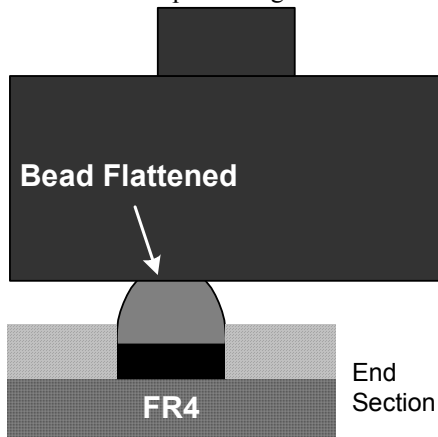


Figure 9: A bead probe flattens when contacted.

Beads are (approximate) hemi-ellipsoidal structures. When a hard, flat surface is pressed onto them, the initial contact is a point with infinite pressure, so the solder must move. As the surface yields, an area begins to form which is basically an ellipse with a semi-major axis A that runs along the length of the bead, and a semi-minor axis B that runs along the width. The area of the ellipse is πAB . The area continues to increase until it is able to support the spring force. Using the yield strength of solder expressed in ounces per square mil (0.08), we see the areas needed to support a force in the following table:

Probe spring force (oz)	Area to support force (mil ²)
2	25
4	50
8	100

The semi-minor axis of a bead is often constrained to the width of the trace it sits upon. If a bead is too small, the surface area needed to support the spring force might be larger than the bead itself, implying that the bead would be catastrophically crushed out over the solder mask. If the bead is overly large, then the surface yield area may not displace enough solder to move oxides.

The semi-minor axis should not exceed 50% of W ($W > 2B$) as shown in Figure 10 as this would imply bead crushing.

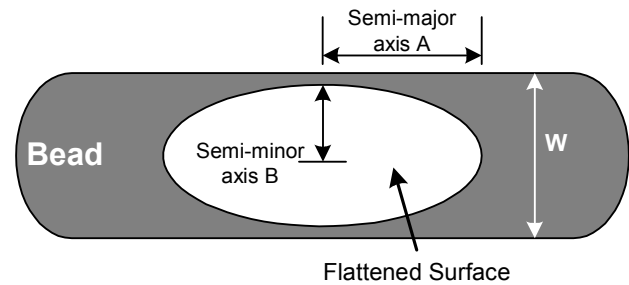


Figure 10: Top view of a flattened bead.

The following table shows semi-major axis lengths needed to support spring forces for some bead widths and forces. For low spring forces, beads must be very small or there will not be much surface yield on the bead. For all beads, the semi-major axis must be smaller than $\frac{1}{2}$ length of the bead, as was true for the semi-minor axis versus width. Again, using the 50% factor, each bead length should be greater than 2 times the semi-major axis length ($L > 2A$).

Bead widths less than 4 mils will be more difficult to build reliably, since the solder mask registration on a correspondingly narrow trace will become a factor. Also, the width to height ratio will become a factor, since the bead must be tall enough to clear the solder mask by several mils. The solder mask itself supports the sides of a bead, but building tall skinny beads may not be reliable.

Spring Force (oz)	Bead Width (mils)	Semi-minor axis B (mils)	Semi-major axis A (mils)
2	3	1.5	5.3
	4	2	4
	5	2.5	3.2
4	4	2	8
	6	3	5.3
	8	4	4
8	4	2	16
	6	3	10.6
	8	4	8

8 Bead Probe Fabrication Experiments

A board containing several types of bead probes was constructed to see how several possible designs would

work. Several dozen beads were photographed, and then sectioned and photographed under a microscope where accurate measurements were made. Both virgin beads and probed beads were measured.

Figure 11 shows a newly minted bead from the top, mounted on one of a pair of differential traces with 4 mil line and 6 mil space. The elliptical area surrounding the bead is flux residue (no-clean process).

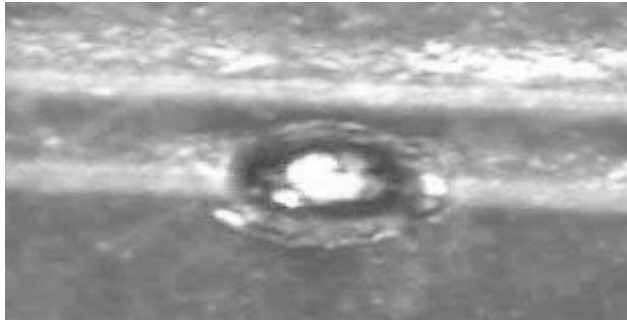


Figure 11: Photo of a virgin bead from the top, on one trace of a differential pair.

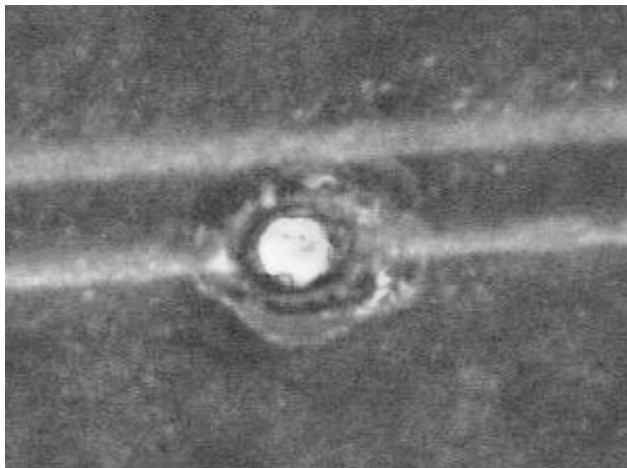


Figure 12: Topside photo of a probed bead. Note flattened surface.

Figure 12 shows a bead that has been probed ten times with an 8-ounce probe. It looked the same after only one probing. The flattened area has a characteristic shine of clean solder. The area is not very elliptical as theory predicts, but the area is commensurate with theory.

Before looking at sectioned beads, see the photo in Figure 13 where a differential pair has been sectioned. Notice the etching and plating effects (CuNiAu plating) have created a trace with over-etched walls and a mushroom cap.

Figure 14 shows a section of a bead. At this point the bead was 2.9 mils tall. Other sections of the same bead had heights ranging from 2.3 to 3.7 mils. The width stayed fairly constant. Figure 15 shows a bead that has been probed. The top surface shows the flattening caused by yielding solder.



Figure 13: Microphotograph of sectioned differential traces.

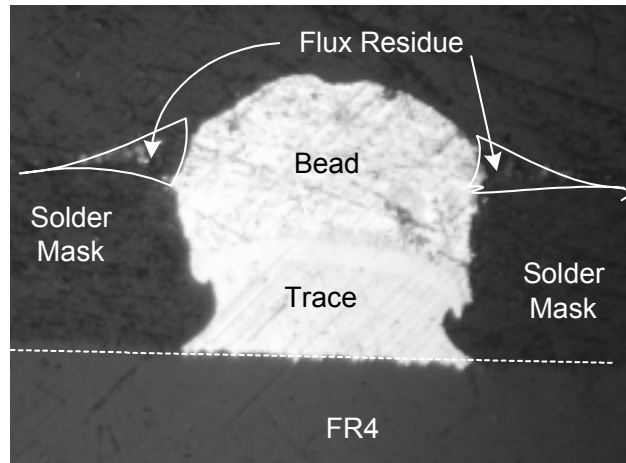


Figure 14: A bead, 2.9 mils tall, and 5.3 mils wide.

Figure 16 shows a bead that was mal-formed due to solder mask mis-registration. In this bead style, the solder mask was deliberately made 1 mil wider than the trace to see if solder would stick to the side of the trace, or leave an empty “gutter”. In some cases, the gutter stayed clear of solder. In this case, the solder mask was misaligned to the left by ½ mil, causing an overall gap of 1 mil on the left side and no space on the right. In this case, solder did flow into the gutter and stick to the side of the trace. This widens the trace in this vicinity by ½ mil, which could affect the characteristic impedance of the line.

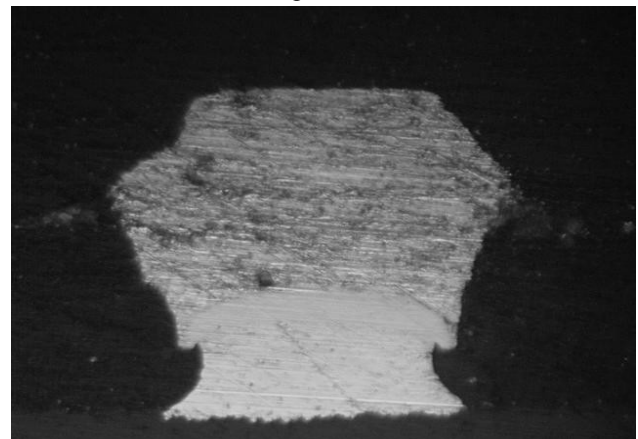


Figure 15: Cross section of a flattened bead.

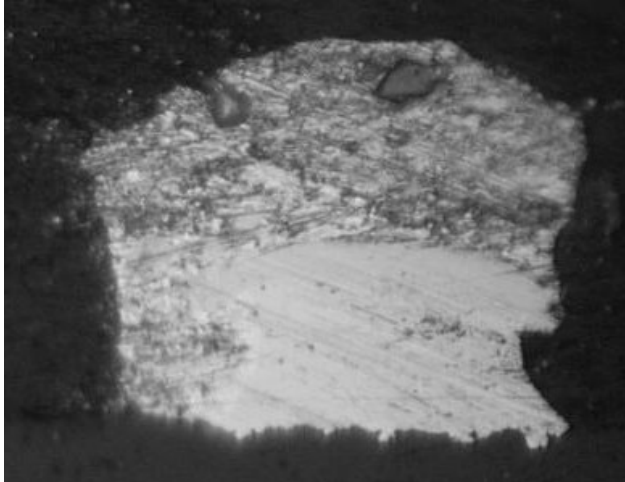


Figure 16: Section of a mal-formed bead due to solder mask mis-registration.

A new set of beads is being produced at this writing, using the process laid out in section 6.2 that does not produce a gutter.

9 Probing Performance

A set of 41 beads of varying styles was checked for DC contact impedance using very accurate 4-wire measurements. Each bead's contact resistance was measured ten times in succession. The mean resistance of all the beads was 11.89 milliohms with a sigma of 1.02 milliohms. This compares very well with standard probe contact resistance. There was very little change in the measurements from first to last measurement. These beads had been manufactured in a no-clean process a month earlier so there had been time for some oxidation to occur. However, this was not a controlled part of this experiment.

A question did arise about the subsequent oxidation of a flattened bead. For example, if a board is tested and found faulty, it will go to a repair process. It is reasonable to expect that the repair process might allow time for a new oxide layer to build up. To see if this was the case, the tested board was "soaked" in 95% humidity at 40 degrees C for 48 hours. (The solder was leaded.) The beads were tested again and found to now have 20.60 milliohms of mean contact resistance with 5.25 milliohms sigma.

This rise in contact impedance is a concern. There are several ways to deal with it. One would be to reflow the board before re-testing (which may have been a result of the repair). Reflowing will restore the original shape of each bead. Second would be to chemically remove the oxide, but this seems impractical. Last is to use "twist probes" that twist (say) 45 degrees while being depressed in their sockets. This causes the flat-face probe to wipe the surface of the bead. At this writing, this last idea is being studied.

Finally, a crude life-test was conducted on the beads. Each was probed and re-measured 500 times. A contact was rated marginal if it ever exceeded 100 milliohms. The earliest a probe became marginal was after 38 cycles with a mean of 280 cycles. One type of bead was particularly small and fragile, especially with respect to 8-ounce probe force. When data for this type of bead was removed, the earliest and mean numbers jumped up to 145 and 332 respectively.

10 High Frequency Characteristics

What is the performance impact of a bead probe at elevated transmission frequencies? We look at this question in the context of single-ended transmission lines.

10.1 Theory

Consider a design that achieves a characteristic impedance of 80 ohms. The trace width is 8 mils, the height above the ground plane is 12 mils and the trace thickness is 1.4 mils. The capacitance of such a line is 1.75 pf/in and the propagation delay is 141 ps/in. Now consider a 15 mil long bead probe situated in the center of a length of this line. The height of this bead probe changes the effective trace thickness. For ease of analysis, assume the height is uniform, although we expect there to be some tapering at either end. The following table shows the theoretical effects of the bead on impedance, capacitance and propagation delay, for several different bead heights.

	Bead height above trace in mils			
	0 (none)	4	5	6
Impedance Z_0 in ohms	80	65	62	60
Capacitance in pf/in	1.75	2.16	2.26	2.36
Inductance in nf/in	11.28	9.17	8.74	8.46
Prop delay in ps/in	141	141	141	141

One approach to modeling this is to divide a transmission line into 15 mil long segments and use the LC model for each segment, based on the 1st column of numbers normalized to 15 mil segments. Pick a segment in the middle and substitute the LC values for a given bead size. Then use a Spice simulator to simulate the effects of the perturbed L and C values.

A second approach is to view the transmission line on either side of the bead as "normal" and the bead as simply a lumped capacitive load in the center of a transmission line (see [JoGr93]). Then analyze the effect. Note the modeled capacitor would be the increment of capacitance from the table minus the "normal" capacitance, and that value needs to be normalized to the 15-mil

length since the table is stated in pf/in (i.e., multiply the bead capacitance minus the normal capacitance by 0.015. The lumped capacitance to analyze would be 6, 7.7 and 9 femtofarads for the 4, 5 and 6 mil beads.

Theory is best backed up with measurements taken from “real” structures. Many factors will interact with the effects of beads and some of these will actually mask the effects of beads, causing one or another theoretical model to be superior for a given situation. The next section explores this.

10.2 Empirical Experiment Setup

A controlled impedance printed circuit board was constructed with several kinds of experimental features included for physical measurements of high-frequency behavior. This board contained 4 major experiments in two groups. The first group was composed of 5 mil traces. The second group was composed of 18 mil traces. Both were designed for 50 ohm characteristic impedances with a tolerance of 10%. Within each group there were 2 subgroups of experimental structures where the measurement access technique was varied. In the first subgroup (the “connector subgroup”) the access was provided with Rosenberger 32K243-40ME3 microwave connectors. In the second (“probe”) subgroup, access was provided by specifically laid-out surface probe points and associated calibration structures. This gave us flexibility to measure and account for the signal-quality effects of the access technology itself.

Within the connector subgroups (of both 5 and 18 mil line experiments) we laid out an “ideal” single-ended trace 3 inches long as a reference trace. Next we laid out a 3-inch trace with a classical 35 mil test point in the center. This would allow us to measure the effects of a standard test point on the characteristic impedance. Next we laid out a 3-inch trace with 3 bead probes in the center, each separated by 3.5 mils. The geometries varied: for the 5 mil line we set $L=20$, $W=7.5$ and $D=13$. For the 18 mil line $L=22.5$, $W=5$ and $D=13$. This meant there was a small gutter around the 5 mil line. For the 18 mil line, the width of the trace far exceeded the width of the bead, which was centered on the trace. Finally, two differential pairs were laid out (only on the 5 mil subgroup) one ideal with no probe access, and one with three beads on each of the pair of traces, offset by 100 mils near the center of the 3-inch run. The differential traces had to be separated by an inch at the ends to accommodate the connectors. This would cause an unavoidable impedance discontinuity.

The reason we chose 3 beads in succession on the traces was because initial simulations predicted that a single bead’s effects would be difficult to measure. The simulations suggested that at least 3 in close proximity would be needed to cause a measurable difference. All the connector subgroup trace lengths were 3 inches.

Within the probe subgroups, we varied trace lengths

and numbers of beads. We had a 3-inch ideal trace (no test point), a 3-inch trace with a standard 35 mil test point and a 3-inch trace with 3 bead probes. These could be compared to the connector subgroup traces to see the discontinuities our instrumentation access would cause. We also laid out 3-inch differential pairs (ideal and with 3 bead probes per pair member) for similar comparisons. Then we laid out traces with centered triples of beads, of lengths 1, 2, 4 and 5 inches in length. We expected the effects of the beads to be most evident on shorter lengths because the attenuating effects of longer traces could become dominant, making the bead effects hard to measure on them. Finally, we laid out several more 3-inch traces with 1, 5 7 and 9 bead probes centered and separated by 3.5 mils each. These allowed us to measure the accumulated effects of beads in the event that a single bead (or even 3) had immeasurable effects, as suggested by simulation. (In practice, we would seldom see more than 1 bead on a trace.)

The measurements were taken using an Agilent E-8362B Vector Network Analyzer (VNA) operating from 10 MHz to 20 GHz and using a 40 GHz probing set. These were used to confirm and adjust models in the Agilent EEsof Advanced Design Simulator system (see <http://eesof.tm.agilent.com/docs/>).

Finally, a total of 4 such boards were made. All four used a no-clean Organic Surface Protected (OSP) process. Two were soldered with common tin/lead solder and two were soldered with lead-free (Sn95.5%/Ag3.9%/Cu0.6%) solder. These were then inspected visually for bead integrity.

10.3 Experimental Results

Visual inspection of the beads showed excellent formation of beads on the 18-mil lines (side one of the board). However, there was a significant solder stencil misalignment problem³ on side two that combined with the somewhat retarded solder affinity of the OSP coated copper that caused the 5-mil lines to have a uniformly different shape. These beads (expected $L=20$) had L about two thirds this long (see Figure 17) causing them to be taller than planned. The beads were still nicely formed but were more steeply hemi-ellipsoidal than expected.⁴ We continued with the high-frequency experiments anyway. The effects of these beads were expected to be smaller than what we had designed.

There is a notable difference in performance between the ideal traces (no test access) and traces with standard 35 mil probe targets. Figure 18 shows a Time Domain Reflectometer (TDR) plot for the 3-inch-long 5 mil ideal trace versus a similar trace with a 35 mil test

³ The amount of misalignment was sufficient to reject a board in normal production. We did not have time to re-run the board.

⁴ This implies these beads would support a smaller spring force.

target at its center. The actual trace impedance is around 44 ohms so there are discontinuities at the point where the signal is injected and observed by the VNA. The ideal trace stays at a fairly constant 44 ohms across the entire length, but the targeted trace has a fairly large drop to around 35 ohms at its center.

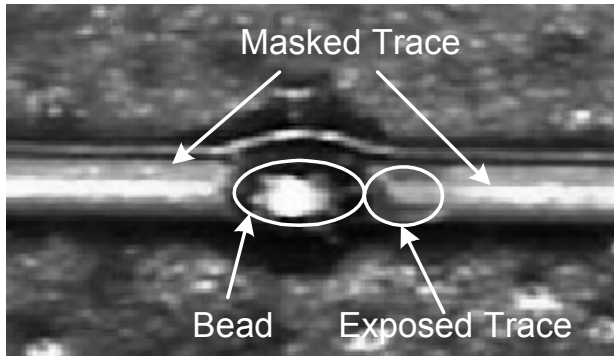


Figure 17: Malformed bead on 5-mil trace due to a correctable solder stencil misalignment.

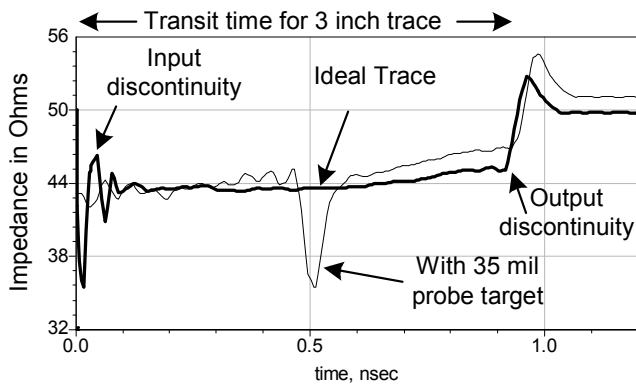


Figure 18: TDR result of ideal 3-inch-long 5 mil trace and 5 mil trace with a standard 35 mil test target.

The Agilent EEsop ADS package is able to convert data from the VNA measurements into Eye Diagrams. Figure 19 shows the Eye for an ideal trace.

Figure 20 shows the Eye for the similar trace with a 35 mil test target at its center. The target causes some reflections which reduce the usable area of the Eye. While the signal is still discernable, a designer would have to factor this test-target-induced signal degradation into the overall degradation budget.

Next, consider the traces with bead probes at their centers. We expected the effects of a single bead to be small, so we analyzed the traces with clusters of beads. Figure 21 shows a TDR plot for an ideal trace, a trace with a 35 mil target and a trace with nine bead probes clustered on it. This plot has been zoomed to show the region where the discontinuities are due to the beads and target. The figures shows the bead probe trace to be almost completely unaffected by the addition of nine

beads, losing about 1 ohm across the span of about 150 picoseconds. This is so close to normal impedance variations due to other factors as to be unnoticeable.

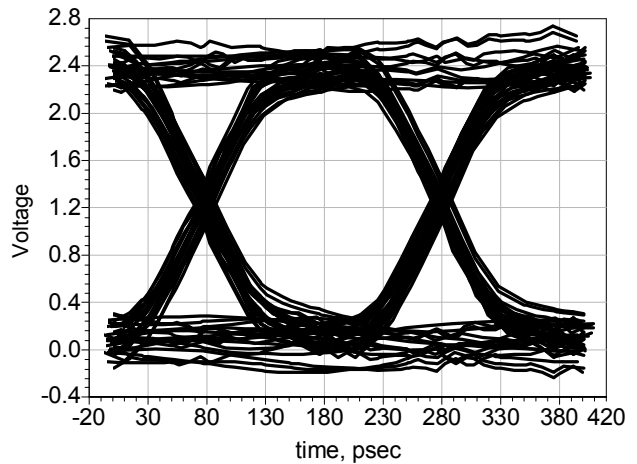


Figure 19: Eye diagram for ideal trace, 100 ps rise time, 5 GB/s, 50 bit random pattern.

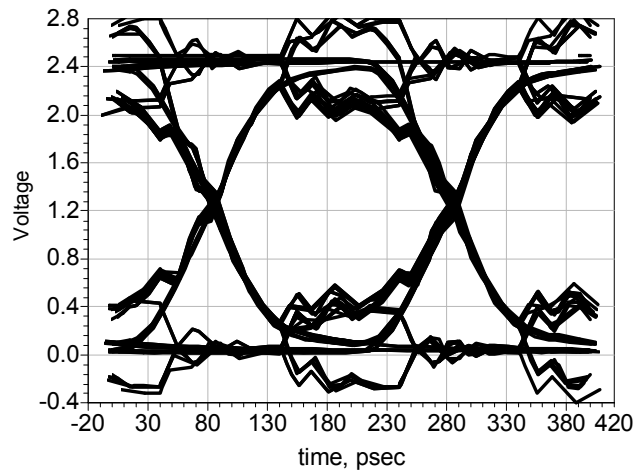


Figure 20: Eye diagram for trace with 35 mil test target, 100 ps rise time, 5 GB/s, 50 bit random pattern.

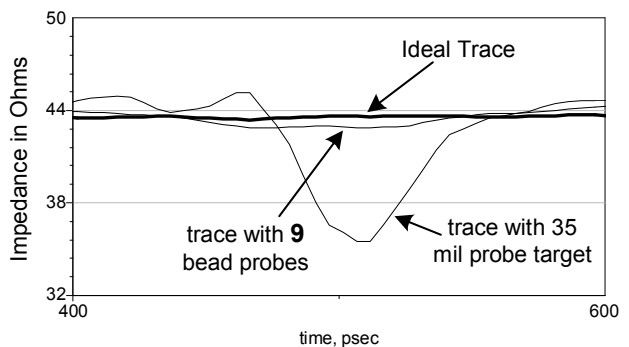


Figure 21: Discontinuity of 35 mil test target versus 5 mil trace with 9 bead probes.

Figure 22 shows the Eye for this trace with nine

beads on it. It is almost identical to the ideal Eye seen in Figure 19.

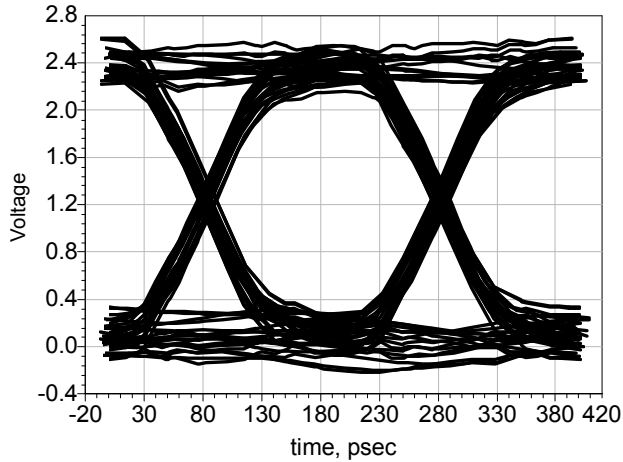


Figure 22: Eye diagram for trace with 9 bead probes, 100 ps rise time, 5 GB/s, 50 bit random pattern.

Beads, even 9 in a row, centered on 18-mil lines were essentially invisible to the measurement hardware up to 20 GHz. These beads were only 28% the width of the trace itself and had no measurable performance effect. We expect that normal process variations in the 18-mil lines themselves swamp out the effects of the beads.

From the data so far extracted, it was found that a good model of a bead is that of a lumped capacitance of about 10 femtofarads on an otherwise ideal transmission line, as theorized in section 10.1. This value of capacitance is quite small and most designs would consider it negligible. Indeed, a single via along a trace path is often modeled as a 100 fF capacitance, ten times the discontinuity as a single bead probe of about 5x20 mils.

Shorter 5-mil traces with 3 beads showed more effects than longer traces. In effect, bead performance effects will only be a factor on very short traces, where there is likely more margin for these effects. Longer traces can also be viewed as high-frequency attenuators, so those frequencies that could be affected by bead probes are already compromised by the length of the trace.

Again using data supplied by the VNA to validate models used in ADS, we simulated the effects of a bead probe on a trace only 0.2 inches in length. The Eye for this appears in Figure 23. This diagram contains both the ideal and beaded trace plots, but it is essentially identical even at an elevated data rate.

11 Conclusion

Bead probes allow for In-Circuit test access on highly dense layouts or gigabit signals and have negligible impact on circuit performance during normal operation. Bead probes allow us to approach an ideal of “layout independent” test point placement which is of great benefit in high-density designs. Bead probes are

easily fabricated with the same solder masking/stenciling steps already widely used, with no unusual or extra steps. Bead probes can be inserted into a design process by generating library models for the layer stack ups of various bead widths, lengths, heights and orientation. One could ask if bead probes might someday supplant conventional probing technology.

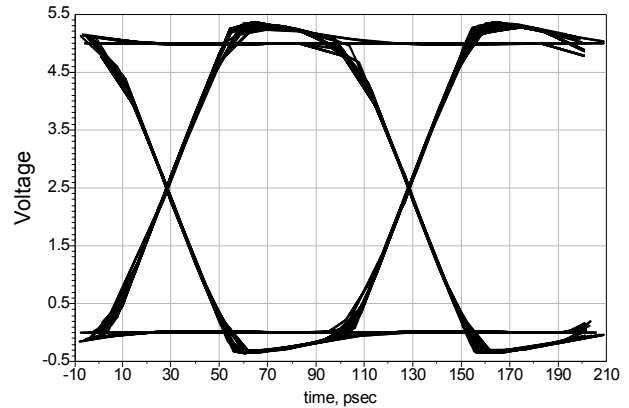


Figure 23: Eye diagram for a 0.2 inch trace with a single bead probe, 50 ps rise time, 10 GB/s, 50 bit random pattern.

12 Acknowledgements

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